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Single Event Effects in High Altitude Aerospace Sensor Applications

There are many advantages to utilizing active electronics versus the passive systems often used in aircraft applications, such as pressure, temperature, and flow sensors. Some of these advantages are increased accuracy, reduced noise, transmission over longer signal paths, and the addition of signal conditioning. With these benefits comes the consideration that high altitude operation will expose the electronics to high-energy neutron solar particle radiation. Without proper design and component selection, this radiation may affect the reliability of measurements from aircraft sensors.

Neutrons exist at high altitudes, created mainly by nuclear activity in the sun. At higher altitudes, there is little protective atmosphere to attenuate these neutrons. Other particles, such as protons and electrons, interact with both the magnetic field and with layers of charged particles found in the Van Allen belts surrounding the earth where these belts provide an effective radiation shield to the earth.

The lack of electrical charge causes neutrons to be relatively unaffected at high altitudes, where the concentration of air molecules is thin. Once within the atmosphere, collisions with oxygen, nitrogen, and water molecules provide a relatively effective shield that attenuates neutron energy as the particles travel to lower altitudes. The attenuated energy remaining in any surviving neutrons typically has insufficient energy at or near the ground to affect electronics.

Since neutrons have no charge to interact, it is impractical to attempt to use manmade shields in aircraft applications where size and weight is crucial. As an example, with the neutron energy typically seen at 70,000 feet above sea level, a neutron can penetrate a three-foot thick block of concrete. Some materials, such as those with high levels of hydrogen (water, polyethylene), can provide attenuation, but the practicality of building a universal shield for all sensors with these materials is usually not achievable.

To prevent electronics from showing upset due to neutron single event effects (SEE), it is possible to either select from components that intrinsically have insignificant response, or provide circuit design to manage any event that does occur. The mechanism of neutron-induced upset will be described in the next section.

Single Event Effects: What the Neutron Does to Electronics

Single Event Effects (SEE) are a result of a collision between a single, energetic particle and active portions of an electronic component. When this collision occurs in a specific location within a component, such as the gate of a transistor, it can induce an electrical event by charge generation, or atom dislocation (see figure on next page).

The collision occurs between an energetic charge-less neutron particle and a semiconductor atomic lattice within a circuit as shown. Energetic particles, such as neutrons impinging on a material, lose their energy in a direct nuclear impact collision.

Three Types of SEE

The result of this collision can be broken down into three types of SEE.

SEU	**Single Event Upset** a permanent change in characteristic
SET	**Single Event Transient** a transient self-extinguishing event
SEL	**Single Event Latch-Up** turning on of parasitic circuit elements that may lead to permanent burnout

As neutrons transfer energy by interacting with the nucleus of lattice atoms, a secondary effect called spallation may throw off secondary particles, such as protons, electrons, lower energy ionizing photons, and lower energy neutrons. These additional particles cause secondary upset and observable changes in performance. The effect of either neutron displacement or spallation-charged particle movement within a critical location of an integrated circuit can alter characteristics leading to discernible phenomena such as gain change, offset change, transient upset or latch-up.

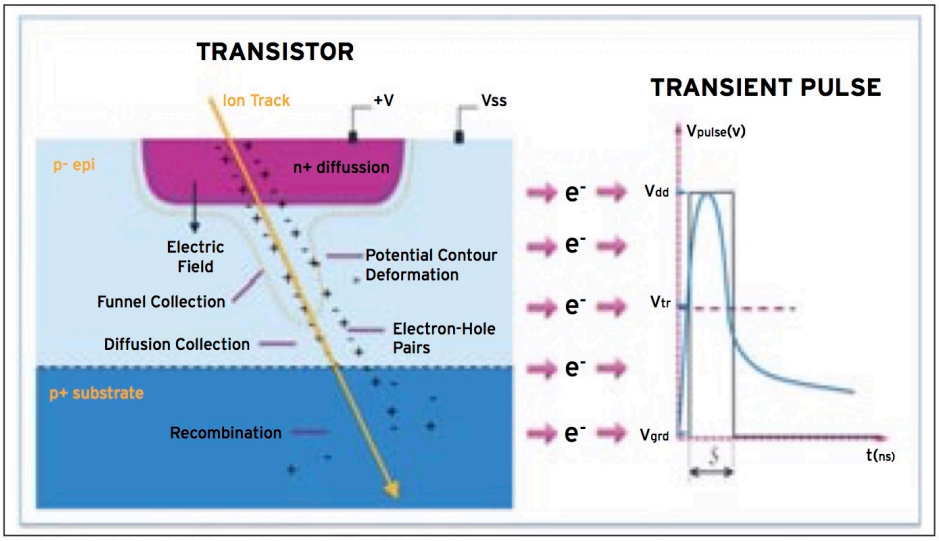
Single Event Upset

Consider the condition where the collision alters the silicon lattice to generate a charge within a circuit's transistor sufficient to cause an effect (this mechanism will be described later). This charge may have the capacity to turn a transistor on, off, or partially on or off. This general condition of altering the circuit performance is classified as SEU.

Single Event Transient Effects

A single event upset that is transient in nature is classified as a single event transient (SET). These can occur where memory cells are refreshed, or a fast transient charge is generated in analog circuit. SET can impact the digital propagation of data, modify analog signals, or trigger a temporary bit flip in memory structures.

Transient upset can be mitigated by appropriate use of low pass filtering to eliminate the high frequency nature of the signal, refreshing a digital memory, or performing error correction. Once an analog signal recovers or the digital signal is refreshed, the SET has concluded and normal device operation resumes.



Neutron collision path in semiconductor lattice

Single Event Latch-Up

Single event latch-up (SEL) may occur in the condition where the generated charge triggers a 4-layer configuration PNPN SCR type parasitic structure to latch in a conducting state. Structures like these can exist in CMOS (complementary metal oxide semiconductor) devices where an ESD (electrostatic discharge) or overvoltage protection circuit is built in. This "SCR" effect can lead to a low impedance conduction path which draws current that can only be recovered with power reset. Without specific current-limiting elements, the circuit may draw excessive levels of current that can damage the device.

This type of SEL can be minimized or eliminated by careful avoidance of designs that include this PNPN structure, inclusion of voltage clamps, or by the use of current-limiting protection circuits.

Determining Susceptibility of a Circuit to SEE

There are several generally accepted methods of characterizing the level of susceptibility of a circuit to SEE. The most direct is to test the circuit in a neutron source with known energy distribution. The term for this measure is *neutron fluence*.

Neutron Fluence Testing. Testing the effect of the fluence on the performance of the device can lead to a statistical characterization of the SEE events and remove repetitive redundancies. Testing can characterize SEU, SET, SEL and SEB events. Standard charts of fluence at differing altitudes and locations around the earth are available from NASA and other organizations.

While testing provides a measure of SEE event characterization, it is time-consuming and costly. Testing may also be subject to variation from device manufacturing process variations, without ample representative samples of the device.

SEE Modeling. A second method of determining susceptibility level of a circuit to SEE is physical analysis of the characteristics of the device. Modeling can consider variations in manufacturing characteristics and, with knowledge of the device physical structure, can provide highly accurate results. While the cost of modeling may not be insignificant, it can be less than that of direct neutron fluence testing.

Linear Energy Transfer (LET). As shown in the figure, energetic ions lose energy through collision generally along a straight track in the material. Attributed to this straight track energy transfer is the term Linear Energy Transfer (LET). Although the energy lost by the ion is not exactly the same as the energy transferred to the material due to re-radiation effects,

the term LET is often used interchangeably with energy loss or stopping power. The level of LET can be used to calculate the effect on the electronic component.

Designing to Mitigate or Prevent SEE

When upset does occur through spallation or direct nuclear collision, several methods are available to mitigate the effect. One method used in analog responding circuits adds a low pass filter to eliminate the effect of generated high frequency transients. Where a memory cell may be involved, the cells can be refreshed with correct patterns or, through error correction methods, a corrected pattern can be restored. Where there is risk of high current latch-up, protective circuits that limit or reset the circuit can be included in a design.

The best method of eliminating single event upset is to provide a design that is not susceptible to the effects. To insure the design is protected from collision or spallation upset, the physical and electrical structure needs to be understood.

Since the upset is in electronic circuits responding to electrical signals, the upset must be an electrical event that causes the upset. This electrical event can be called a movement or generation of electrical charge. If we can know the minimum charge required to upset an electronic component, such as a transistor, design choices can be made which limit charge build to a level below the upset threshold.

Upset Energy Minimum Threshold

The critical charge, Q_{crit}, is the amount of charge required to cause a MOS transistor gate to be turned on or off. This is device dependent and is therefore unique to the geometry and threshold of an Integrated Circuit (IC). Determining this charge will define the minimum threshold incident of neutron energy to cause upset within the electronics.

Using an example of a gate length, L = 1.125 µm, and width, W = 1.0 µm. The capacitance of the gate is given by:

$$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{t_G}$$

where ε_0 is the permeability of free space, ε_r is the dielectric constant of the gate oxide, A is the gate area, and t_G is the gate oxide thickness. Solving with t_G = 10 nm gives:

$$C = \left(8.85 \cdot 10^{-12} \tfrac{F}{m}\right)(3.9) \cdot \frac{(1 \cdot 10^{-6} m)(1.125 \cdot 10^{-6} m)}{10 \cdot 10^{-9} m} = 3.9 fF$$

Therefore, the critical charge for upset is:

$$Q_{crit} = CV_{threshold}$$

For a CMOS transistor, a gate threshold can typically be $V_{threshold}$ = 2V on a 5 volt operating system. Thus:

$$Q_{crit} = (3.9 \cdot 10^{-15} fF)(2V) = 7.8 fC = 0.0078 pC$$

The next step is to calculate the equivalent LET to produce the critical charge of 0.0078 pC. With a gate area,

Single Event Effects

Single event effects (SEE) can potentially result in catastrophic consequences for aircraft. SEE was investigated as a factor contributing to the failure suffered by Qantas Airlines Flight 72 en route from Perth to Singapore on October 7, 2008. When incorrect data entered the flight control systems of the Airbus A330-303, the plane suddenly and severely pitched downwards, rapidly descending 650 feet in about 20 seconds before the pilots were able to regain control. The incident caused significant injuries to 110 passengers and nine crew members. Although SEE was not specifically cited as a cause, the increased risk of potential error from high altitude SEE was noted in the final report.

Breaking Moore's Law

The technological capacity to produce increasingly small transistors has simultaneously created its own threatening challenge. These densely packed nano-transistors are vulnerable to smaller bursts of neutron charge, exposing them to the possibility of more frequent errors.

t_{GA} = 10 µm, the equivalent charge transfer rate Q′ = 0.00078 pC/µm.

$$Q' = \frac{LET}{97} \cdot \frac{1}{MeV \cdot cm^2 / mg}$$

[from Reference 1]

The energy absorbed from a neutron to generate the charge can then be calculated from:

$$LET = \left(0.00078 \tfrac{pC}{\mu m}\right)\left(97 \tfrac{Mn}{pC}\right) \cdot 1 MeV \cdot cm^2 / mg = 0.076 MeV \cdot cm^2 / mg$$

If the neutron fluence energy can be made to be less than this amount, then no upset can occur.

Conclusion

It is possible with known levels of neutron fluence causing single event effects in high altitude aerospace sensors to select appropriate components that eliminate or reduce SEE. Prediction of the upset as well as effectiveness of prevention can be determined by understanding the physical configuration of electronic components exposed to high altitude neutron radiation. Units may be tested, but an accurate estimation can also be calculated to know the effects of radiation and eliminate or reduce SEE. For those neutron flux conditions capable of creating a critical level of upset, the probability of an event can be made small by selecting the geometry and complexity of the electronics included.

If the predicted radiation is still considered a risk, mitigation can be added to minimize any probability of significant events.

This article was written by Bob Guziak, VP of Engineering, Hydra-Electric (Burbank, CA). For more information, visit ***http://info.hotims.com/69513-500****.*

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